AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method comprising:

forming a gate dielectric above a surface of the substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region; and

forming a first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure.

2. (Currently Amended) ~~The method of claim 1,~~ A method comprising:

forming a gate dielectric above a surface of the substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region; and

forming a first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure, wherein forming the first dopant-depleted region includes implanting a counter-dopant into the edge region of the doped-poly gate structure adjacent the gate dielectric, and forming the second dopant-depleted region includes implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure.

3. (Original) The method of claim 2, the method further comprising:

implanting the counter-dopant at an angle α with respect to a direction perpendicular to the surface, wherein the angle α is in a range of about 7°-45°;

rotating the substrate through at least one of approximately 90° (approximately $\pi/2$ radians), approximately 180° (approximately π radians), and approximately 270° (approximately $3\pi/2$ radians); and

implanting the counter-dopant at the angle α with respect to the direction perpendicular to the surface.

4. (Currently Amended) ~~The method of claim 1, the method further comprising~~ A method comprising:

forming a gate dielectric above a surface of the substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region;

forming a first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure; and

forming a photoresist mask defining a source/drain extension (SDE) adjacent the doped-poly gate structure.

5. (Original) The method of claim 2, the method further comprising forming a photoresist mask defining a source/drain extension (SDE) adjacent the doped-poly gate structure.

6. (Original) The method of claim 3, the method further comprising forming a photoresist mask defining a source/drain extension (SDE) adjacent the doped-poly gate structure.

7. (Previously Presented) The method of claim 1, wherein forming the first and second dopant-depleted regions includes depleting the edge region of the doped-poly gate structure adjacent the gate dielectric by forming depleting dielectric spacers adjacent the doped-poly gate structure and depleting the substrate under the edge region of the doped-poly gate structure by forming the depleting dielectric spacers.

8. (Previously Presented) The method of claim 2, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure and the substrate under the edge region includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure and the substrate under the edge region, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×1014 ions/cm2 to about 1.0×1015 ions/cm2 at an implant energy ranging from about 0.2-5 keV.

9. (Previously Presented) The method of claim 3, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure and the substrate under the edge region includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure and the substrate under the edge region, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×1014 ions/cm2 to about 1.0×1015 ions/cm2 at an implant energy ranging from about 0.2-5 keV.

10. (Currently Amended) ~~The method of claim 1~~, <u>A method comprising:</u>

<u>forming a gate dielectric above a surface of the substrate;</u>

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region; and

forming a first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure, wherein forming the first dopant-depleted region in the edge region of the doped-poly gate structure includes forming the first dopant-depleted region to have a depth from the edge of the doped-poly gate structure, the depth of the first dopant-depleted region ranging from about 50 Å-100 Å.

11. (Previously Presented) A method comprising:

forming a gate dielectric above a surface of a substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region;

forming a source/drain extension (SDE) adjacent the doped-poly gate structure; and

forming a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure.

12. (Currently Amended) ~~The method of claim 11~~ A method comprising:

forming a gate dielectric above a surface of a substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region;

forming a source/drain extension (SDE) adjacent the doped-poly gate structure; and

forming a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure, wherein forming the dopant-depleted-poly region includes implanting a counter-dopant into the edge region of the doped-poly gate structure adjacent the gate dielectric, and forming the dopant-depleted-SDE region includes implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure.

13. (Original) The method of claim 12, the method further comprising:

implanting the counter-dopant at an angle α with respect to a direction perpendicular to the surface, wherein the angle α is in a range of about 7°-45°;

rotating the substrate through at least one of approximately 90° (approximately $\pi/2$ radians), approximately 180° (approximately π radians), and approximately 270° (approximately $3\pi/2$ radians); and

implanting the counter-dopant at the angle α with respect to the direction perpendicular to the surface.

14. (Currently Amended) ~~The method of claim 11, further comprising~~ A method comprising:

forming a gate dielectric above a surface of a substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region;

forming a source/drain extension (SDE) adjacent the doped-poly gate structure;

forming a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure; and

forming a photoresist mask defining the SDE adjacent the doped-poly gate structure.

15. (Original) The method of claim 12, the method further comprising forming a photoresist mask defining the SDE adjacent the doped-poly gate structure.

16. (Original) The method of claim 13, the method further comprising forming a photoresist mask defining the SDE adjacent the doped-poly gate structure.

17. (Previously Presented) The method of claim 11, wherein forming the dopant-depleted-poly region includes depleting the edge region of the doped-poly gate structure adjacent the gate dielectric by forming depleting dielectric spacers adjacent the doped-poly gate structure, and forming the dopant-depleted-SDE region includes depleting the SDE in the substrate under the edge region of the doped-poly gate structure by forming the depleting dielectric spacers above the SDE.

18. (Original) The method of claim 12, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure, and implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure includes implanting the one of phosphorus, arsenic, boron and boron fluoride into the substrate under the

edge region of the doped-poly gate structure, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×1014 ions/cm2 to about 1.0×1015 ions/cm2 at an implant energy ranging from about 0.2-5 keV.

19. (Original) The method of claim 13, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure, and implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure includes implanting the one of phosphorus, arsenic, boron and boron fluoride into the substrate under the edge region of the doped-poly gate structure, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×1014 ions/cm2 to about 1.0×1015 ions/cm2 at an implant energy ranging from about 0.2-5 keV.

20. (Currently Amended) ~~The method of claim 11~~, <u>A method comprising:</u>

<u>forming a gate dielectric above a surface of a substrate;</u>

<u>forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region;</u>

<u>forming a source/drain extension (SDE) adjacent the doped-poly gate structure; and</u>

<u>forming a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure,</u> wherein forming the dopant-depleted-poly region in the edge region of the doped-poly gate structure includes forming the dopant-depleted-poly region to have a first depth from the edge of the doped-poly gate structure, the first depth ranging from

about 50 Å-100 Å, and forming the dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure includes forming the dopant-depleted-SDE region to have a second depth from the surface of the substrate, the second depth ranging from about 50 Å-100 Å.

21. (Withdrawn) An MOS transistor having a reduced Miller capacitance, the MOS transistor formed by a method comprising:

forming a gate dielectric above a surface of the substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region; and

forming a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric.

22. (Withdrawn) The MOS transistor of claim 21, wherein forming the dopant-depleted-poly region includes implanting a counter-dopant into the edge region of the doped-poly gate structure adjacent the gate dielectric.

23. (Withdrawn) The MOS transistor of claim 22, the method further comprising:

implanting the counter-dopant at an angle α with respect to a direction perpendicular to the surface, wherein the angle α is in a range of about 7°-45°;

rotating the substrate through at least one of approximately 90° (approximately $\pi/2$ radians), approximately 180° (approximately π radians), and approximately 270° (approximately $3\pi/2$ radians); and

implanting the counter-dopant at the angle α with respect to the direction perpendicular to the surface.

24. (Withdrawn) The MOS transistor of claim 21, the method further comprising:

forming a photoresist mask defining a source/drain extension (SDE) adjacent the doped-poly gate structure.

25. (Withdrawn) The MOS transistor of claim 22, the method further comprising:

forming a photoresist mask defining a source/drain extension (SDE) adjacent the doped-poly gate structure.

26. (Withdrawn) The MOS transistor of claim 23, the method further comprising:

forming a photoresist mask defining a source/drain extension (SDE) adjacent the doped-poly gate structure.

27. (Withdrawn) The MOS transistor of claim 21, wherein forming the dopant-depleted-poly region includes depleting the edge region of the doped-poly gate structure adjacent the gate dielectric by forming depleting dielectric spacers adjacent the doped-poly gate structure.

28. (Withdrawn) The MOS transistor of claim 22, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

29. (Withdrawn) The MOS transistor of claim 23, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

30. (Withdrawn) The MOS transistor of claim 21, wherein forming the dopant-depleted-poly region in the edge region of the doped-poly gate structure includes forming the dopant-depleted-poly region to have a depth from an edge of the doped-poly gate structure, the depth of the dopant-depleted-poly region ranging from about 50 Å-100 Å.

31. (Withdrawn) An MOS transistor having a reduced Miller capacitance, the MOS transistor formed by a method comprising:

forming a gate dielectric above a surface of the substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region;

forming a source/drain extension (SDE) adjacent the doped-poly gate structure; and

forming a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure.

32. (Withdrawn) The MOS transistor of claim 31, wherein forming the dopant-depleted-poly region includes implanting a counter-dopant into the edge region of the doped-poly gate structure adjacent the gate dielectric, and forming the dopant-depleted-SDE region includes implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure, reducing the Miller capacitance of the edge region of the doped-poly gate structure of the MOS transistor.

33. (Withdrawn) The MOS transistor of claim 32, the method further comprising:

implanting the counter-dopant at an angle α with respect to a direction perpendicular to the surface, wherein the angle α is in a range of about 7°-45°;

rotating the substrate through at least one of approximately 90° (approximately π/2 radians), approximately 180° (approximately π radians), and approximately 270° (approximately 3π/2 radians); and

implanting the counter-dopant at the angle α with respect to the direction perpendicular to the surface.

34. (Withdrawn) The MOS transistor of claim 31, the method further comprising:

forming a photoresist mask defining the SDE adjacent the doped-poly gate structure.

35. (Withdrawn) The MOS transistor of claim 32, the method further comprising:

forming a photoresist mask defining the SDE adjacent the doped-poly gate structure.

36. (Withdrawn) The MOS transistor of claim 33, the method further comprising:

forming a photoresist mask defining the SDE adjacent the doped-poly gate structure.

37. (Withdrawn) The MOS transistor of claim 31, wherein forming the dopant-depleted-poly region includes depleting the edge region of the doped-poly gate structure adjacent the gate dielectric by forming depleting dielectric spacers adjacent the doped-poly gate structure, and forming the dopant-depleted-SDE region includes depleting the SDE in the substrate under the edge region of the doped-poly gate structure by forming the depleting dielectric spacers above the SDE.

38. (Withdrawn) The MOS transistor of claim 32, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure, and implanting the counter-dopant into the substrate under the edge region of the doped-poly gate

structure includes implanting the one of phosphorus, arsenic, boron and boron fluoride into the substrate under the edge region of the doped-poly gate structure, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

39. (Withdrawn) The MOS transistor of claim 33, wherein implanting the counter-dopant into the edge region of the doped-poly gate structure includes implanting one of phosphorus, arsenic, boron and boron fluoride into the edge region of the doped-poly gate structure, and implanting the counter-dopant into the substrate under the edge region of the doped-poly gate structure includes implanting the one of phosphorus, arsenic, boron and boron fluoride into the substrate under the edge region of the doped-poly gate structure, a dose of the one of phosphorus, arsenic, boron and boron fluoride ranging from about 1.0×10^{14} ions/cm^2 to about 1.0×10^{15} ions/cm^2 at an implant energy ranging from about 0.2-5 keV.

40. (Withdrawn) The MOS transistor of claim 31, wherein forming the dopant-depleted-poly region in the edge region of the doped-poly gate structure includes forming the dopant-depleted-poly region to have a first depth from the edge of the doped-poly gate structure, the first depth ranging from about 50 Å-100 Å, and forming the dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure includes forming the dopant-depleted-SDE region to have a second depth from the surface of the substrate, the second depth ranging from about 50 Å-100 Å.

41. (Withdrawn) An MOS transistor comprising:

a gate dielectric above a surface of a substrate;

a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge and an edge region; and

a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric.

42. (Withdrawn) The MOS transistor of claim 41, wherein the dopant-depleted-poly region has a depth from the edge of the doped-poly gate structure, the depth of the dopant-depleted-poly region ranging from about 50 Å-100 Å.

43. (Withdrawn) The MOS transistor of claim 41, wherein the MOS transistor has a reduced Miller capacitance in the edge region of the doped-poly gate structure of the MOS transistor due to the dopant-depleted-poly region.

44. (Withdrawn) An MOS transistor comprising:

a gate dielectric above a surface of a substrate;

a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge and an edge region;

a source/drain extension (SDE) adjacent the doped-poly gate structure;

a dopant-depleted-poly region in the edge region of the doped-poly gate structure adjacent the gate dielectric; and

a dopant-depleted-SDE region in the substrate under the edge region of the doped-poly gate structure.

45. (Withdrawn) The MOS transistor of claim 44, wherein the dopant-depleted-poly region has a first depth from the edge of the doped-poly gate structure, the first depth ranging from about 50 Å-100 Å, and the dopant-depleted-SDE region has a second depth from the edge of the doped-poly gate structure, the second depth ranging from about 50 Å-100 Å.

46. (Withdrawn) The MOS transistor of claim 44, wherein the MOS transistor has a reduced Miller capacitance in the edge region of the doped-poly gate structure of the MOS transistor due to the dopant-depleted-poly region and the dopant-depleted-SDE region.

47. (Previously Presented) A method, comprising:

forming a gate dielectric above a surface of a semiconductor substrate;

forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region; and

forming a first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure by:

implanting a counter-dopant into the edge region of the doped-poly gate structure adjacent the gate dielectric; and

forming depleting dielectric spacers adjacent the doped-poly gate structure.